

**AFFILIATED INSTITUTIONS**  
**ANNA UNIVERSITY, CHENNAI**  
**REGULATIONS - 2009**  
**CURRICULUM II TO IV SEMESTERS (FULL TIME)**  
**M.E. APPLIED ELECTRONICS**

**SEMESTER II**

SL. NO	COURSE CODE	COURSE TITLE	L	T	P	C
<b>THEORY</b>						
1	AP9221	<u>Analysis and Design of Analog Integrated Circuits</u>	3	0	0	3
2	<b>AP9222</b>	<u>Computer Architecture and Parallel Processing</u>	3	0	0	3
3	AP9223	<u>Digital Control Engineering</u>	3	0	0	3
4	AP9224	<u>Embedded Systems</u>	3	0	0	3
5	E2	Elective II	3	0	0	3
6	E3	Elective III	3	0	0	3
<b>PRACTICAL</b>						
7	AP9227	<u>Electronics Design Lab II</u>	0	0	4	2
<b>TOTAL</b>			<b>18</b>	<b>0</b>	<b>4</b>	<b>20</b>

**SEMESTER III**

SL. NO	COURSE CODE	COURSE TITLE	L	T	P	C
<b>THEORY</b>						
1	E4	Elective IV	3	0	0	3
2	E5	Elective V	3	0	0	3
3	E6	Elective VI	3	0	0	3
<b>PRACTICAL</b>						
4	AP9234	Project Work (Phase I)	0	0	12	6
<b>TOTAL</b>			<b>9</b>	<b>0</b>	<b>12</b>	<b>15</b>

**SEMESTER IV**

SL. NO	COURSE CODE	COURSE TITLE	L	T	P	C
<b>PRACTICAL</b>						
1	AP9241	Project Work (Phase II)	0	0	24	12
<b>TOTAL</b>			<b>0</b>	<b>0</b>	<b>24</b>	<b>12</b>

Total no.of credits to be earned for the award of Degree 21+20+15+12 = 68

**LIST OF ELECTIVES  
M.E. APPLIED ELECTRONICS**

<b>SL. NO</b>	<b>COURSE CODE</b>	<b>COURSE TITLE</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
1	AP9251	<u>Digital Image Processing</u>	3	0	0	3
2	AP9252	<u>Neural Networks and Its Applications</u>	3	0	0	3
3	AP9253	<u>Robotics</u>	3	0	0	3
4	VL9211	<u>DSP Integrated Circuits</u>	3	0	0	3
5	VL9261	<u>ASIC Design</u>	3	0	0	3
6	AP9260	<u>Design and Analysis of Algorithms</u>	3	0	0	3
7	NE9251	<u>Reliability Engineering</u>	3	0	0	3
8	AP9256	<u>Electromagnetic Interference and Compatibility in System Design</u>	3	0	0	3
9	CP9212	<u>High Performance Computer Networks</u>	3	0	0	3
10	AP9258	<u>RF system Design</u>	3	0	0	3
11	VL9252	<u>Low Power VLSI Design</u>	3	0	0	3
12	VL9253	<u>VLSI Signal Processing</u>	3	0	0	3
13	VL9254	<u>Analog VLSI Design</u>	3	0	0	3
14	VL9221	<u>CAD for VLSI Circuits</u>	3	0	0	3
15	AP9259	<u>Hardware Software Co-design</u>	3	0	0	3
16		Special Elective	3	0	0	3

**UNIT I MODELS FOR INTEGRATED CIRCUIT ACTIVE DEVICES 9**

Depletion region of a PN junction – large signal behavior of bipolar transistors- small signal model of bipolar transistor- large signal behavior of MOSFET- small signal model of the MOS transistors- short channel effects in MOS transistors – weak inversion in MOS transistors- substrate current flow in MOS transistor.

**UNIT II CIRCUIT CONFIGURATION FOR LINEAR IC 9**

Current sources, Analysis of difference amplifiers with active load using BJT and FET, supply and temperature independent biasing techniques, voltage references. Output stages: Emitter follower, source follower and Push pull output stages.

**UNIT III OPERATIONAL AMPLIFIERS 9**

Analysis of operational amplifiers circuit, slew rate model and high frequency analysis, Frequency response of integrated circuits: Single stage and multistage amplifiers, Operational amplifier noise

**UNIT IV ANALOG MULTIPLIER AND PLL 9**

Analysis of four quadrant and variable trans conductance multiplier, voltage controlled oscillator, closed loop analysis of PLL, Monolithic PLL design in integrated circuits: Sources of noise- Noise models of Integrated-circuit Components – Circuit Noise Calculations – Equivalent Input Noise Generators – Noise Bandwidth – Noise Figure and Noise Temperature

**UNIT V ANALOG DESIGN WITH MOS TECHNOLOGY 9**

MOS Current Mirrors – Simple, Cascode, Wilson and Widlar current source – CMOS Class AB output stages – Two stage MOS Operational Amplifiers, with Cascode, MOS Telescopic-Cascode Operational Amplifier – MOS Folded Cascode and MOS Active Cascode Operational Amplifiers

**TOTAL: 45PERIODS****REFERENCES:**

1. Gray, Meyer, Lewis, Hurst, "Analysis and design of Analog IC's", Fourth Edition, Willey International, 2002.
2. Behzad Razavi, "Principles of data conversion system design", S.Chand and company ltd, 2000
3. Nandita Dasgupta, Amitava Dasgupta,"Semiconductor Devices, Modelling and Technology", Prentice Hall of India pvt. ltd, 2004.
4. Grebene, Bipolar and MOS Analog Integrated circuit design", John Wiley & sons,Inc.,2003.
5. Phillip E.Allen Douglas R. Holberg, "CMOS Analog Circuit Design", Second Edition- Oxford University Press-2003



**UNIT I PRINCIPLES OF CONTROLLERS 9**

Review of frequency and time response analysis and specifications of control systems, need for controllers, continuous time compensations, continuous time PI, PD, PID controllers, digital PID controllers.

**UNIT II SIGNAL PROCESSING IN DIGITAL CONTROL 9**

Sampling, time and frequency domain description, aliasing, hold operation, mathematical model of sample and hold, zero and first order hold, factors limiting the choice of sampling rate, reconstruction.

**UNIT III MODELING AND ANALYSIS OF SAMPLED DATA CONTROL SYSTEM 9**

Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems, stability of digital control systems, Jury's stability test, state variable concepts, first companion, second companion, Jordan canonical models, discrete state variable models, elementary principles.

**UNIT IV DESIGN OF DIGITAL CONTROL ALGORITHMS 9**

Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane.

**UNIT V PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS 9**

Algorithm development of PID control algorithms, software implementation, implementation using microprocessors and microcontrollers, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems.

**TOTAL: 45 PERIODS****REFERENCES :**

1. M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997.
2. John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill, 1995.
3. Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996.

**UNIT I EMBEDDED PROCESSORS 9**

Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded Computing system design, Embedded system design process- Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration, Formalism for System Design- Structural Description, Behavioural Description, Design Example: Model Train Controller, ARM processor-processor and memory organization.

**UNIT II EMBEDDED PROCESSOR AND COMPUTING PLATFORM 9**

Data operations, Flow of Control, SHARC processor- Memory organization, Data operations, Flow of Control, parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory devices, Input/output devices, Component interfacing, designing with microprocessor development and debugging, Design Example : Alarm Clock. Hybrid Architecture

**UNIT III NETWORKS 9**

Distributed Embedded Architecture- Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link supports, Ethernet, Myrinet, Internet, Network-Based design- Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller.

**UNIT IV REAL-TIME CHARACTERISTICS 9**

Clock driven Approach, weighted round robin Approach, Priority driven Approach, Dynamic Versus Static systems, effective release times and deadlines, Optimality of the Earliest deadline first (EDF) algorithm, challenges in validating timing constraints in priority driven systems, Off-line Versus On-line scheduling.

**UNIT V SYSTEM DESIGN TECHNIQUES 9**

Design Methodologies, Requirement Analysis, Specification, System Analysis and Architecture Design, Quality Assurance, Design Example: Telephone PBX- System Architecture, Ink jet printer- Hardware Design and Software Design, Personal Digital Assistants, Set-top Boxes.

**TOTAL: 45 PERIODS****REFERENCES:**

1. Wayne Wolf, "Computers as Components: Principles of Embedded Computing System Design", Morgan Kaufman Publishers.
2. Jane.W.S. Liu, "Real-Time systems", Pearson Education Asia.
3. C. M. Krishna and K. G. Shin, "Real-Time Systems", McGraw-Hill, 1997
4. Frank Vahid and Tony Givargis, "Embedded System Design: A Unified Hardware/Software Introduction", John Wiley & Sons.

**AP9227**

**ELECTRONICS DESIGN LAB II**

**L T P C  
0 0 4 2**

1. System design using PLL
2. System design using CPLD
3. Alarm clock using embedded micro controller
4. Model train controller using embedded micro controller
5. Elevator controller using embedded micro controller
6. Simulation of Non adaptive Digital Control System using MAT LAB control system toolbox
7. Simulation of Adaptive Digital Control System using MAT LAB control system toolbox

**AP9251**

**DIGITAL IMAGE PROCESSING**

**L T P C  
3 0 0 3**

**UNIT I DIGITAL IMAGE FUNDAMENTALS 9**

Elements of digital image processing systems, Vidicon and Digital Camera working principles, Elements of visual perception, brightness, contrast, hue, saturation, Mach Band effect, Image sampling, Quantization, Dither, Two dimensional mathematical preliminaries.

**UNIT II IMAGE TRANSFORMS 9**

1D DFT, 2D transforms - DFT, DCT, Discrete Sine, Walsh, Hadamard, Slant, Haar, KLT, SVD, Wavelet transform.

**UNIT III IMAGE ENHANCEMENT AND RESTORATION 9**

Histogram modification, Noise distributions, Spatial averaging, Directional Smoothing, Median, Geometric mean, Harmonic mean, Contraharmonic and Yp mean filters . Design of 2D FIR filters. Image restoration - degradation model, Unconstrained and Constrained restoration, Inverse filtering-removal of blur caused by uniform linear motion, Wiener filtering, Geometric transformations-spatial transformations, Gray Level interpolation. .

**UNIT IV IMAGE SEGMENTATION AND RECOGNITION 9**

Image segmentation - Edge detection, Edge linking and boundary detection, Region growing, Region splitting and Merging, Image Recognition - Patterns and pattern classes, Matching by minimum distance classifier, Matching by correlation., Neural networks-Backpropagation network and training, Neural network to recognize shapes.

**UNIT V IMAGE COMPRESSION 9**

**Need for data compression, Huffman, Run Length Encoding, Shift codes, Arithmetic coding, Vector Quantization, Block Truncation Coding, Transform coding, JPEG standard, JPEG 2000, EZW, SPIHT, MPEG.**

**TOTAL: 45 PERIODS**

## REFERENCES:

1. Rafael C. Gonzalez, Richard E. Woods, "Digital Image Processing", Pearson Education, Inc., Second Edition, 2004
2. Anil K. Jain, "Fundamentals of Digital Image Processing", Prentice Hall of India, 2002.
3. Rafael C. Gonzalez, Richard E. Woods, Steven Eddins, "Digital Image Processing using MATLAB", Pearson Education, Inc., 2004.
4. D.E. Dudgeon and R.M. Mersereau, "Multidimensional Digital Signal Processing", Prentice Hall Professional Technical Reference, 1990.
5. William K. Pratt, "Digital Image Processing", John Wiley, New York, 2002.
6. Milan Sonka et al, "Image Processing, Analysis and Machine Vision", Brookes/Cole, Vikas Publishing House, 2nd edition, 1999;
7. Sid Ahmed, M.A., "Image Processing Theory, Algorithms and Architectures", McGrawHill, 1995.

AP9252

NEURAL NETWORKS AND ITS APPLICATIONS

L T P C  
3 0 0 3

### UNIT I BASIC LEARNING ALGORITHMS 9

Biological Neuron – Artificial Neural Model - Types of activation functions – Architecture: Feedforward and Feedback – Learning Process: Error Correction Learning –Memory Based Learning – Hebbian Learning – Competitive Learning - Boltzman Learning – Supervised and Unsupervised Learning – Learning Tasks: Pattern Space – Weight Space – Pattern Association – Pattern Recognition – Function Approximation – Control – Filtering - Beamforming – Memory – Adaptation - Statistical Learning Theory – Single Layer Perceptron – Perceptron Learning Algorithm – Perceptron Convergence Theorem – Least Mean Square Learning Algorithm – Multilayer Perceptron – Back Propagation Algorithm – XOR problem – Limitations of Back Propagation Algorithm.

### UNIT II RADIAL-BASIS FUNCTION NETWORKS AND SUPPORT VECTOR MACHINES RADIAL BASIS FUNCTION NETWORKS 9

Cover's Theorem on the Separability of Patterns - Exact Interpolator – Regularization Theory – Generalized Radial Basis Function Networks - Learning in Radial Basis Function Networks - Applications: XOR Problem – Image Classification. Support Vector Machines: Optimal Hyperplane for Linearly Separable Patterns and Nonseparable Patterns – Support Vector Machine for Pattern Recognition – XOR Problem -  $\epsilon$ -insensitive Loss Function – Support Vector Machines for Nonlinear Regression

### UNIT III COMMITTEE MACHINES 9

Ensemble Averaging - Boosting – Associative Gaussian Mixture Model – Hierarchical Mixture of Experts Model(HME) – Model Selection using a Standard Decision Tree – A Priori and Postpriori Probabilities – Maximum Likelihood Estimation – Learning Strategies for the HME Model - EM Algorithm – Applications of EM Algorithm to HME Model

### NEURODYNAMICS SYSTEMS

Dynamical Systems – Attractors and Stability – Non-linear Dynamical Systems- Lyapunov Stability – Neurodynamical Systems – The Cohen-Grossberg Theorem.







**UNIT III DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 9**  
 FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects -Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

**UNIT IV DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES 9**  
 DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory architectures. Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.

**UNIT V ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN 9**  
 Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor, DCT processor and Interpolator as case studies. Cordic algorithm.

**TOTAL: 45 PERIODS**

**REFERENCES:**

1. Lars Wanhammer, "DSP Integrated Circuits", 1999 Academic press, New York
2. A.V.Oppenheim et.al, "Discrete-time Signal Processing", Pearson Education, 2000.
3. Emmanuel C. Ifeachor, Barrie W. Jervis, " Digital signal processing – A practical approach", Second Edition, Pearson Education, Asia.
4. Keshab K.Parhi, "VLSI Digital Signal Processing Systems design and Implementation", John Wiley & Sons, 1999.

**VL9261 ASIC DESIGN L T P C  
3 0 0 3**

**UNIT I INTRODUCTION TO ASICs, CMOS LOGIC AND ASIC LIBRARY DESIGN 9**  
 Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture .

**UNIT II PROGRAMMABLE ASICs, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 9**  
 Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

**UNIT III PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY 9**  
 Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

**UNIT IV LOGIC SYNTHESIS, SIMULATION AND TESTING 9**  
 Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

**UNIT V ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING 9**  
 System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.

**TOTAL: 45 PERIODS**

**REFERENCES:**

1. M.J.S .Smith, "Application Specific Integrated Circuits, Addison -Wesley Longman Inc., 1997.
2. Farzad Nekoogar and Faranak Nekoogar, From ASICs to SOCs: A Practical Approach, Prentice Hall PTR, 2003.
3. Wayne Wolf, FPGA-Based System Design, Prentice Hall PTR, 2004.
4. R. Rajsuman, System-on-a-Chip Design and Test. Santa Clara, CA: Artech House Publishers, 2000.
5. F. Nekoogar. Timing Verification of Application-Specific Integrated Circuits (ASICs). Prentice Hall PTR, 1999.

**AP9260 DESIGN AND ANALYSIS OF ALGORITHMS L T P C**  
**3 0 0 3**

**UNIT I INTRODUCTION 9**  
 Polynomial and Exponential algorithms, big "oh" and small "oh" notation, exact algorithms and heuristics, direct / indirect / deterministic algorithms, static and dynamic complexity, stepwise refinement.

**UNIT II DESIGN TECHNIQUES 9**  
 Subgoals method, working backwards, work tracking, branch and bound algorithms for traveling salesman problem and knapsack problem, hill climbing techniques, divide and conquer method, dynamic programming, greedy methods.

**UNIT III SEARCHING AND SORTING 9**  
 Sequential search, binary search, block search, Fibonacci search, bubble sort, bucket sorting, quick sort, heap sort, average case and worst case behavior

**UNIT IV GRAPH ALGORITHMS 9**  
 Minimum spanning, tree, shortest path algorithms, R-connected graphs, Even's and Kleitman's algorithms, max-flow min cut theorem, Steiglitz's link deficit algorithm.

**UNIT V SELECTED TOPICS 9**  
 NP Completeness Approximation Algorithms, NP Hard Problems, Strassen's Matrix Multiplication Algorithms, Magic Squares, Introduction To Parallel Algorithms and Genetic Algorithms, Monte-Carlo Methods, Amortised Analysis.

**TOTAL: 45PERIODS**

## REFERENCES:

1. Sara Baase, "Computer Algorithms : Introduction to Design and Analysis", Addison Wesley, 1988.
2. T.H.Cormen, C.E.Leiserson and R.L.Rivest, "Introduction to Algorithms", Mc Graw Hill, 1994.
3. E.Horowitz and S.Sahni, "Fundamentals of Computer Algorithms", Galgotia Publications, 1988.
4. D.E.Goldberg, "Genetic Algorithms : Search Optimization and Machine Learning", Addison Wesley, 1989.

**NE9251**

**RELIABILITY ENGINEERING**

**L T P C**  
**3 0 0 3**

### **UNIT I            PROBABILITY PLOTTING AND LOAD-STRENGTH INTERFERENCE**

**9**

Statistical distribution , statistical confidence and hypothesis testing ,probability plotting techniques – Weibull, extreme value ,hazard, binomial data; Analysis of load – strength interference , Safety margin and loading roughness on reliability.

### **UNIT II            RELIABILITY PREDICTION, MODELLING AND DESIGN**

**9**

Statistical design of experiments and analysis of variance Taguchi method, Reliability prediction, Reliability modeling, Block diagram and Fault tree Analysis ,petric Nets, State space Analysis, Monte carlo simulation, Design analysis methods – quality function deployment, load strength analysis, failure modes, effects and criticality analysis.

### **UNIT III            ELECTRONICS AND SOFTWARE SYSTEMS RELIABILITY**

**9**

Reliability of electronic components, component types and failure mechanisms, Electronic system reliability prediction, Reliability in electronic system design; software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces.

### **UNIT IV            RELIABILITY TESTING AND ANALYSIS**

**9**

Test environments, testing for reliability and durability, failure reporting, Pareto analysis, Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modeling, reliability demonstration, reliability growth monitoring.

### **UNIT V            MANUFACTURE AND RELIABILITY MAQNAGEMENT**

**9**

Control of production variability, Acceptance sampling, Quality control and stress screening, Production failure reporting; preventive maintenance strategy, Maintenance schedules, Design for maintainability, Integrated reliability programmes , reliability and costs, standard for reliability, quality and safety, specifying reliability, organization for reliability.

**TOTAL: 45 PERIODS**

## REFERENCES:

1. Patrick D.T. O'Connor, David Newton and Richard Bromley, Practical Reliability Engineering, Fourth edition, John Wiley & Sons, 2002
2. David J. Klinger, Yoshinao Nakada and Maria A. Menendez, Von Nostrand Reinhold, New York, "AT & T Reliability Manual", 5th Edition, 1998.
3. Gregg K. Hobbs, "Accelerated Reliability Engineering - HALT and HASS", John Wiley & Sons, New York, 2000.
4. Lewis, "Introduction to Reliability Engineering", 2nd Edition, Wiley International, 1996.

**AP9256**

### **ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY IN SYSTEM DESIGN**

**L T P C  
3 0 0 3**

#### **UNIT I EMI/EMC CONCEPTS 9**

EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

#### **UNIT II EMI COUPLING PRINCIPLES 9**

Conducted, radiated and transient coupling; Common ground impedance coupling ; Common mode and ground loop coupling ; Differential mode coupling ; Near field cable to cable coupling, cross talk ; Field to cable coupling ; Power mains and Power supply coupling.

#### **UNIT III EMI CONTROL TECHNIQUES 9**

Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control.

#### **UNIT IV EMC DESIGN OF PCBS 9**

Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations.

#### **UNIT V EMI MEASUREMENTS AND STANDARDS 9**

Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.

**TOTAL: 45 PERIODS**

## REFERENCES:

1. V.P.Kodali, "Engineering EMC Principles, Measurements and Technologies", IEEE Press, Newyork, 1996.
2. Henry W.Ott., "Noise Reduction Techniques in Electronic Systems", A Wiley Inter Science Publications, John Wiley and Sons, Newyork, 1988.
3. Bernhard Keiser, "Principles of Electromagnetic Compatibility", 3<sup>rd</sup> Ed, Artech house, Norwood, 1986.
4. C.R.Paul, "Introduction to Electromagnetic Compatibility", John Wiley and Sons, Inc, 1992.
5. Don R.J.White Consultant Incorporate, "Handbook of EMI/EMC", Vol I-V, 1988.

**UNIT I INTRODUCTION 9**

Review of OSI, TCP/IP; Multiplexing, Modes of Communication, Switching, Routing. SONET – DWDM – DSL – ISDN – BISDN, ATM.

**UNIT II MULTIMEDIA NETWORKING APPLICATIONS 9**

Streaming stored Audio and Video – Best effort service – protocols for real time interactive applications – Beyond best effort – scheduling and policing mechanism – integrated services – RSVP- differentiated services.

**UNIT III ADVANCED NETWORKS CONCEPTS 9**

VPN-Remote-Access VPN, site-to-site VPN, Tunneling to PPP, Security in VPN. MPLS- operation, Routing, Tunneling and use of FEC, Traffic Engineering, MPLS based VPN, overlay networks-P2P connections.

**UNIT IV TRAFFIC MODELLING 8**

Little's theorem, Need for modeling , Poisson modeling and its failure, Non- poisson models, Network performance evaluation.

**UNIT V NETWORK SECURITY AND MANAGEMENT 10**

Principles of cryptography – Authentication – integrity – key distribution and certification – Access control and: fire walls – attacks and counter measures – security in many layers. Infrastructure for network management – The internet standard management framework – SMI, MIB, SNMP, Security and administration – ASN.1

**TOTAL:45 PERIODS****REFERENCES:**

1. J.F. Kurose & K.W. Ross, "Computer Networking- A top down approach featuring the internet", Pearson, 2<sup>nd</sup> edition, 2003.
2. Walrand .J. Varatya, High performance communication network, Morgan Kauffman – Harcourt Asia Pvt. Ltd. 2<sup>nd</sup> Edition, 2000.
3. LEOM-GarCIA, WIDJAJA, "Communication networks", TMH seventh reprint 2002.
4. Aunurag kumar, D. MAnjunath, Joy kuri, "Communication Networking", Morgan Kaufmann Publishers, 1ed 2004.
5. Hersent Gurle & petit, "IP Telephony, packet Pored Multimedia communication Systems", Pearson education 2003.
6. Fred Halsall and Lingana Gouda Kulkarni, "Computer Networking and the Internet" fifth edition, Pearson education
7. Nader F.Mir ,Computer and Communication Networks, first edition.
8. Larry I.Peterson & Bruce S.David, "Computer Networks: A System Approach"- 1996

<b>UNIT I</b>	<b>CMOS PHYSICS, TRANSCIVER SPECIFICATIONS AND ARCHITECTURES</b>	<b>9</b>
	CMOS: Introduction to MOSFET Physics – Noise: Thermal, shot, flicker, popcorn noise Transceiver Specifications: Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link Transceiver Architectures: Receiver: Homodyne, Heterodyne, Image reject, Low IF Architectures – Transmitter: Direct up conversion, Two step upconversion	
<b>UNIT II</b>	<b>IMPEDANCE MATCHING AND AMPLIFIERS</b>	<b>9</b>
	S-parameters with Smith chart – Passive IC components - Impedance matching networks Amplifiers: Common Gate, Common Source Amplifiers – OC Time constants in bandwidth estimation and enhancement – High frequency amplifier design Low Noise Amplifiers: Power match and Noise match – Single ended and Differential LNAs – Terminated with Resistors and Source Degeneration LNAs.	
<b>UNIT III</b>	<b>FEEDBACK SYSTEMS AND POWER AMPLIFIERS</b>	<b>9</b>
	Feedback Systems: Stability of feedback systems: Gain and phase margin, Root-locus techniques – Time and Frequency domain considerations – Compensation Power Amplifiers: General model – Class A, AB, B, C, D, E and F amplifiers – Linearisation Techniques – Efficiency boosting techniques – ACPR metric – Design considerations	
<b>UNIT IV</b>	<b>PLL AND FREQUENCY SYNTHESIZERS</b>	<b>9</b>
	PLL: Linearised Model – Noise properties – Phase detectors – Loop filters and Charge pumps Frequency Synthesizers: Integer-N frequency synthesizers – Direct Digital Frequency synthesizers	
<b>UNIT V</b>	<b>MIXERS AND OSCILLATORS</b>	<b>9</b>
	Mixer: characteristics – Non-linear based mixers: Quadratic mixers – Multiplier based mixers: Single balanced and double balanced mixers – subsampling mixers Oscillators: Describing Functions, Colpitts oscillators – Resonators – Tuned Oscillators – Negative resistance oscillators – Phase noise	
		<b>TOTAL: 45 PERIODS</b>

**TEXT BOOKS:**

1. T.Lee, "Design of CMOS RF Integrated Circuits", Cambridge, 2004
2. B.Razavi, "RF Microelectronics", Pearson Education, 1997
3. Jan Crols, Michiel Steyaert, "CMOS Wireless Transceiver Design", Kluwer Academic Publishers, 1997
4. B.Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill, 2001.



**UNIT I POWER DISSIPATION IN CMOS 9**

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices- Basic principle of low power design.

**UNIT II POWER OPTIMIZATION 9**

Logical level power optimization – Circuit level low power design – Circuit techniques for reducing power consumption in adders and multipliers.

**UNIT III DESIGN OF LOW POWER CMOS CIRCUITS 9**

Computer Arithmetic techniques for low power systems – Reducing power consumption in memories – Low power clock, Interconnect and layout design – Advanced techniques – Special techniques

**UNIT IV POWER ESTIMATION 9**

Power estimation techniques – Logic level power estimation – Simulation power analysis – Probabilistic power analysis.

**UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER 9**

Synthesis for low power –Behavioral level transforms- Software design for low power -

**TOTAL : 45 PERIODS****REFERENCES:**

1. K.Roy and S.C. Prasad , LOW POWER CMOS VLSI circuit design, Wiley,2000
2. Dimitrios Soudris, Chirstian Pignet, Costas Goutis, DESIGNING CMOS CIRCUITS FOR LOW POWER, Kluwer,2002
3. J.B. Kuo and J.H Lou, Low voltage CMOS VLSI Circuits, Wiley 1999.
4. A.P.Chandrakasan and R.W. Brodersen, Low power digital CMOS design, Kluwer,1995.
5. Gary Yeap, Practical low power digital VLSI design, Kluwer,1998.
6. Abdellatif Bellaouar,Mohamed.I. Elmasry, Low power digital VLSI design,s Kluwer, 1995.
7. James B. Kuo, Shin – chia Lin, Low voltage SOI CMOS VLSI Devices and Circuits. John Wiley and sons, inc 2001

**UNIT I INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS 9**

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

**UNIT II RETIMING, ALGORITHMIC STRENGTH REDUCTION 9**

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

**UNIT III FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS 9**

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

**UNIT IV SCALING, ROUND-OFF NOISE, BIT-LEVEL ARITHMETIC ARCHITECTURES 9**

Scaling and round-off noise – scaling operation, round-off noise, state variable description of digital filters, scaling and round-off noise computation, round-off noise in pipelined IIR filters, Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

**UNIT V NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING 9**

Numerical strength reduction – subexpression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

**TOTAL : 45 PERIODS**

**REFERENCES:**

1. Keshab K. Parhi, “ VLSI Digital Signal Processing Systems, Design and implementation “, Wiley, Interscience, 2007.
2. U. Meyer – Baese, “ Digital Signal Processing with Field Programmable Gate Arrays”, Springer, Second Edition, 2004

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**ANALOG VLSI DESIGN**

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**UNIT I BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW-VOLTAGE SIGNAL PROCESSING 9**

Mixed-Signal VLSI Chips-Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques-Super MOS Transistor- Primitive Analog Cells-Linear Voltage-Current Converters-MOS Multipliers and Resistors-CMOS, Bipolar and Low-Voltage BiCMOS Op-Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.

**UNIT II BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT -MODE SIGNAL PROCESSING AND NEURAL INFORMATION PROCESSING 9**

Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched-Current Data Converters-Practical Considerations in SI Circuits Biologically-Inspired Neural Networks - Floating - Gate, Low-Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-Contrast Sensitive Silicon Retina.

**UNIT III SAMPLED-DATA ANALOG FILTERS, OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS 9**

First-order and Second SC Circuits-Bilinear Transformation - Cascade Design-Switched-Capacitor Ladder Filter-Synthesis of Switched-Current Filter- Nyquist rate A/D Converters-Modulators for Over sampled A/D Conversion-First and Second Order and Multibit Sigma-Delta Modulators-Interpolative Modulators –Cascaded Architecture-Decimation Filters-mechanical, Thermal, Humidity and Magnetic Sensors-Sensor Interfaces.

**UNIT IV DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS 9**

Fault modelling and Simulation - Testability-Analysis Technique-Ad Hoc Methods and General Guidelines-Scan Techniques-Boundary Scan-Built-in Self Test-Analog Test Buses-Design for Electron -Beam Testability-Physics of Interconnects in VLSI-Scaling of Interconnects-A Model for Estimating Wiring Density-A Configurable Architecture for Prototyping Analog Circuits.

**UNIT V STATISTICAL MODELING AND SIMULATION, ANALOG COMPUTER-AIDED DESIGN AND ANALOG AND MIXED ANALOG-DIGITAL LAYOUT 9**

Review of Statistical Concepts - Statistical Device Modeling- Statistical Circuit Simulation-Automation Analog Circuit Design-automatic Analog Layout-CMOS Transistor Layout-Resistor Layout-Capacitor Layout-Analog Cell Layout-Mixed Analog -Digital Layout.

**TOTAL : 45 PERIODS**

**REFERENCES:**

1. Mohammed Ismail, Terri Fief, "Analog VLSI signal and Information Processing ", McGraw-Hill International Editons, 1994.
2. Malcom R.Haskard, Lan C.May, "Analog VLSI Design - NMOS and CMOS ", Prentice Hall, 1998.
3. Randall L Geiger, Phillip E. Allen, " Noel K.Strader, VLSI Design Techniques for Analog and Digital Circuits ", Mc Graw Hill International Company, 1990.
4. Jose E.France, Yannis Tsvividis, "Design of Analog-Digital VLSI Circuits for Telecommunication and signal Processing ", Prentice Hall, 1994

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**CAD FOR VLSI CIRCUITS**

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**UNIT I VLSI DESIGN METHODOLOGIES 9**

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.



